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A high-efficiency positive buck–boost converter with three-mode selection circuit and soft start circuit

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Abstract. Positive Buck-Boost converters are considered the optimal choice for battery-powered applications that require high power conversion efficiency and extend battery life. The converter offers versatility in processing input voltages over a wide range thanks to its three operating modes: Boost, Buck, and Buck-Boost (Bck-Bst) while maximizing battery capacity. The efficiency of the converter can be severely affected by a severe ripple in the output voltage and current when transitioning between modes. To reduce the output instability and output ripple during operation, a three-mode selection circuit that uses a very small delay between mode transitions is proposed to minimize the above effects. The proposed chip was designed and implemented on CMOS 0.18 µm process. In addition, a high peak efficiency of 95.6 % can be achieved under the conditions of a wide input range of 2.5 V - 5 V.

Keywords: Three-Mode Selection, DC-DC Converter, Soft Start, Integrated Power Management.

Classification numbers: 4.1.1, 4.1.2.

1. INTRODUCTION

With the increasing use of battery-powered devices, efficient power management is essential to long battery life [1, 2]. Positive Buck-Boost converters are well-suited for this purpose due to their wide input and output voltage range [3 - 8]. These converters operate in three modes Boost, Buck, and Bck-Bst depending on the relationship between V_{IN} and V_{OUT}. Specifically, Boost mode is used when $V_{IN} < V_{OUT}$, Buck mode when $V_{IN} > V_{OUT}$, and Bck-Bst mode when the two are nearly equal. High efficiency across all modes is critical, yet certain converter architectures [9 - 11] face challenges due to complex control requirements involving multiple converter stages and internal oscillators, often resulting in unstable or interrupted operation. Other approaches, like the reverse Buck-Boost in [12, 13], operate continuously in Buck-Boost mode but suffer from high switching currents, increasing device stress. The design in [14] avoids Buck-Boost mode entirely, but switching between Buck and Boost modes introduces significant output ripple and reduced efficiency. Digital control methods [15] offer improved voltage stability through duty cycle overlap yet still struggle with efficiency. This paper proposes a positive Buck-Boost converter that achieves high efficiency across all three

modes by enabling fast, low-latency mode transitions [16]. The proposed design minimizes conduction and switching losses, ensures smooth operation, and includes a soft-start circuit to suppress inrush current and voltage overshoot, thereby improving system reliability.

2. CONVERTER STRUCTURE

A positive Buck-Boost converter, as shown in Figure 1, is a type of switching power supply that can either Boost or Buck an input voltage to produce a regulated output voltage, even if the input voltage fluctuates wildly. The converter runs in the Boost mode when V_{IN} is less than V_{OUT}. Switch S_1 is always switched ON and switch S_2 is always switched OFF. The power switches S_3 and S_4 are controlled along lines 3 and 4 to create this mode. Conversely, in the Buck mode, when V_{IN} exceeds V_{OUT}, switch S_4 is permanently ON and switch S_3 is permanently OFF. The stability of the output voltage is maintained by alternately switching switches S_1 and S_2 along lines 1 and 2. The converter switches to the Bck-Bst mode when V_{IN} is equal to or close to V_{OUT}. In this mode, all switches operate in two groups (S_1-S_3) and (S_2-S_4) to regulate the induction cycle (charging, discharging) along lines 5 and 6. According to the preceding description, the switching action of the power switch and control circuit enables the converter to adapt to changing input circumstances and provide regulated output.

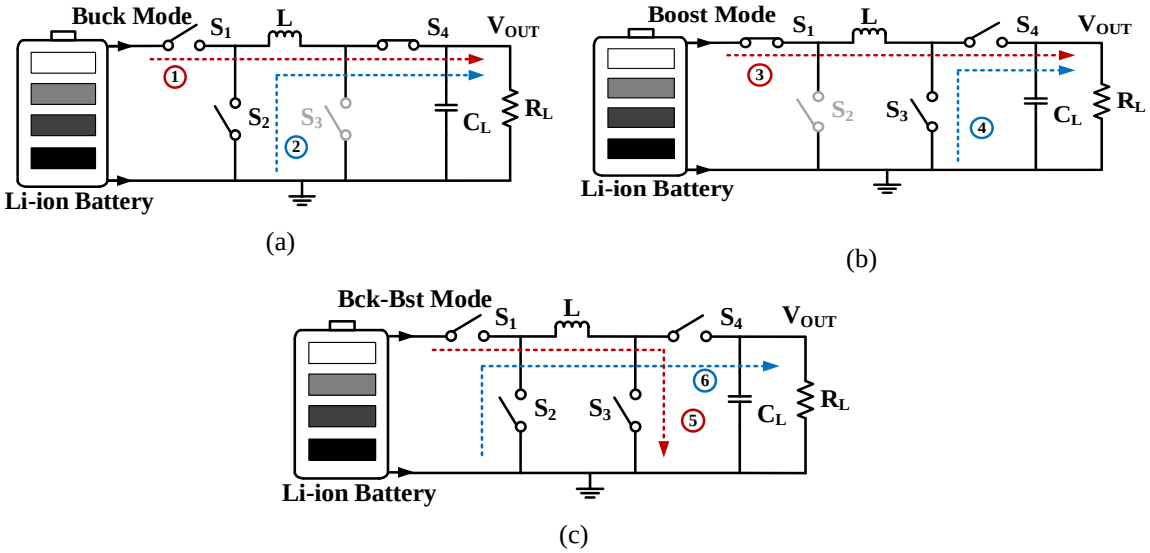

Figure 1. Operational principles of the positive Buck-Boost converter (a) Buck mode (b) Boost mode (c) Bck-Bst mode.

Figure 2 illustrates the block diagram of the proposed system, which includes a control circuit and a power stage. The power stage consists of four on-chip switches ($M_{1,2,3,4}$) with larger transistor sizes to reduce leakage current and on-resistance (R_{on}), improving power conversion efficiency. The control circuit comprises a pulse generator, ramp generator, soft-start circuit, and a three-mode selection circuit. This selection circuit quickly and automatically determines the operating mode by comparing V_{IN} and V_{OUT}, and generates control signals HS_I, LS_I, HS_O, and LS_O accordingly. This enables smooth transitions between Boost, Buck, and Bck-Bst modes, minimizing switching and conduction losses. A soft-start circuit is also included to enhance accuracy and limit inrush current during startup.

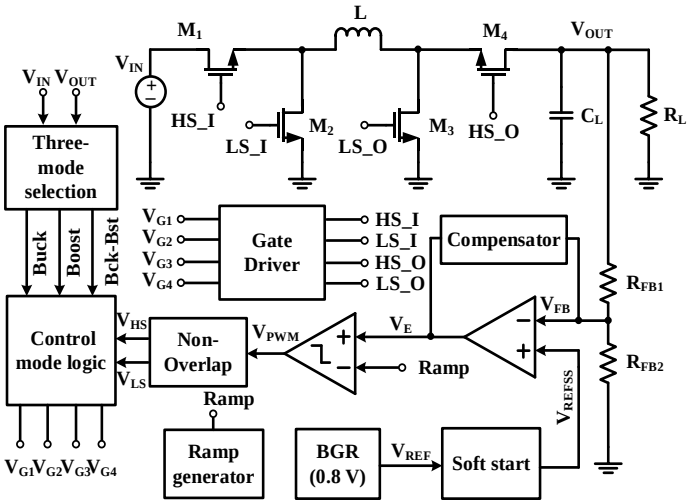

Figure 2. The figure illustrates the block diagram of the proposed system.

3. CIRCUIT DESIGN

3.1. Three-mode selection circuit

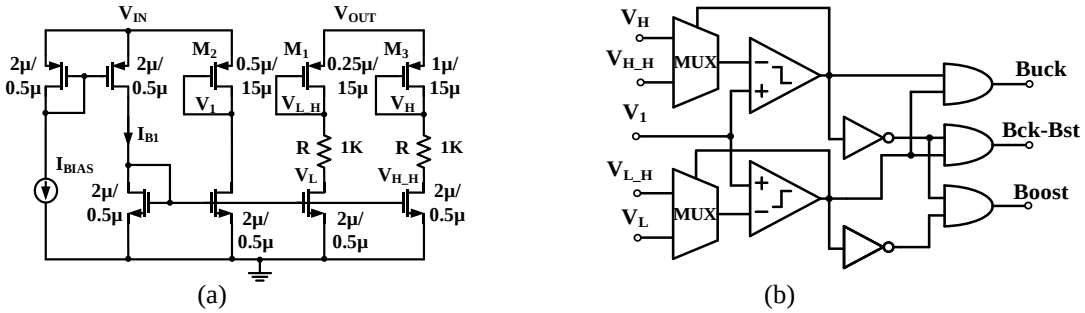

Figure 3. Proposed three-mode selection circuit (a) voltage converter block; (b) mode selection block.

In practice, the input voltage often has a slight slope and may fluctuate, while the bandgap reference voltage can also vary, leading to instability during mode transitions. This can increase leakage current through the switching transistors, reducing efficiency and affecting output voltage regulation. To address this, reference [17] proposes a fixed output architecture to stabilize mode switching. However, this approach lacks flexibility and is unsuitable for systems with variable output. Alternatively, reference [15] introduces a digital controller to monitor and manage converter operation. However, this approach can't work when faced with the challenge of handling high load currents. To meet the dual objective of wide load range operation and high performance, the three-mode selection circuit shown in Figure 3 is proposed. It consists of two main blocks: a voltage converter and a mode selector. The voltage converter processes V_{OUT} and V_{IN} to generate reference signals (V_H, V_L, V_1), where V_L is set lower than the V_H. The mode selector then determines the appropriate operating mode based on these values. As illustrated in Figure 4, V_{OUT} is converted to the V_H, V_{H_H}, V_L, and V_{L_H}, while V_{IN} is converted to the V_1. If the V_1 is below the V_L, the converter operates in Boost mode. When the V_1 lies between the V_L and V_H, the converter enters Bck-Bst mode, capable of either increasing or decreasing the

voltage. If the V_1 exceeds the V_H, the converter switches to Buck mode. To ensure stability and avoid erratic transitions due to minor voltage fluctuations, hysteresis thresholds (V_R) are introduced. For example, transitioning from Bck-Bst to Buck requires V_1 to surpass V_H, while returning requires it to drop below V_{H_H}. Similarly, the V_L and V_{L_H} control the transitions between Boost and Bck-Bst modes. These hysteresis levels are determined by equations (1 - 5), which depend on the MOSFET's W/L ratio, bias current I_{B1}, mobility (μ_P), gate capacitance (C_{ox}), and threshold voltage (V_{TH}). The inclusion of this circuit significantly enhances system adaptability and stability, allowing reliable mode switching under varying input conditions while maintaining optimal performance.

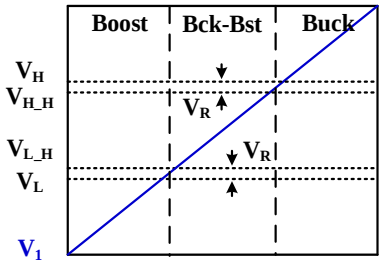

Figure 4. Three-mode operation diagram.

$$V_H = V_{OUT} - |V_{TH}| - \sqrt{\frac{2I_{B1}}{\mu_P C_{ox}(W/L)_{M_3}}} \qquad V_{H\_H} = V_{OUT} - |V_{TH}| - \sqrt{\frac{2I_{B}}{\mu_P C_{ox}(W} \quad (1) \quad - V_R \qquad (2)$$

(3)

$$V_L = V_{OUT} - |V_{TH}| - \sqrt{\frac{2I_{B1}}{\mu_P C_{ox}(W/L)_{M_1}}}$$

$$V_{L\_H} = V_{OUT} - |V_{TH}| - \sqrt{\frac{2I_{B1}}{\mu_P C_{ox}(W/L)_{M_1}}} + V_R \qquad (4)$$

$$V_1 = V_{VIN} - |V_{TH}| - \sqrt{\frac{2I_{B1}}{\mu_P C_{ox}(W/L)_{M_2}}} \qquad (5)$$

State 1: $V_1 < V_L < V_{L\_H} < V_{H\_H} < V_H$

In state 1, where V_{IN} is significantly lower than V_{OUT}. In this mode, the converter operates in Boost mode, both the Buck and Bck-Bst signals are low, and the boost signal is high.

State 2: $V_L < V_{L\_H} < V_1 < V_{H\_H} < V_H$

In state 2, where V_{IN} is close to or equal to V_{OUT}. In this case, the converter operates in Bck-Bst mode, the Boost and Buck signals become low, and the Bck-Bst signal becomes high.

State 3: $V_L < V_{L\_H} < V_{H\_H} < V_H < V_1$

The V_{IN} is greater than V_{OUT} in this state, indicating that the converter operates in Buck mode. As a result, the Boost and Bck-Bst signals become low while the Buck signal becomes high.

3.2. Soft start circuit

During startup, the converter often experiences an inrush current, which is an abrupt surge that can negatively affect key components such as power transistors, feedback circuits, and batteries. This sudden spike in current or voltage may disrupt normal operation and degrade overall system performance [18]. To address this issue, a soft-start circuit is introduced to gradually ramp up the output voltage from 0 to the desired level in a controlled manner. As shown in Figure 5, the proposed soft-start circuit includes a comparator, a 2-to-1 multiplexer (Mux 2_1), and a small soft-start capacitor (C_{SS}). The detailed schematic of the comparator and Mux 2_1 is illustrated in Figure 6. Initially, when the ENB signal is low, the capacitor C_{SS} remains uncharged ($V_C = 0$), the Select signal is 0, and V_{REFSS} is 0, preventing the converter from operating. When ENB goes high, C_{SS} begins to charge slowly through the I_{BIAS} current source. As V_C increases and exceeds the reference threshold (V_{REF}), the comparator switches state, selecting V_{REF} as the main reference voltage ($V_{REFSS} = V_{REF}$), allowing the converter to start operating [19]. The soft-start time (t_{SS}) can be calculated using equation (6), which depends on the bias current (I_{BIAS}), the soft-start capacitor (C_{SS}), and the reference voltage (V_{REF}).

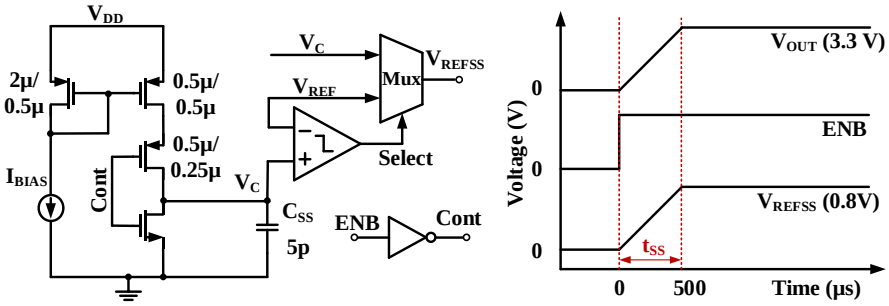

Figure 5. Proposed soft start circuit and the starting sequence.

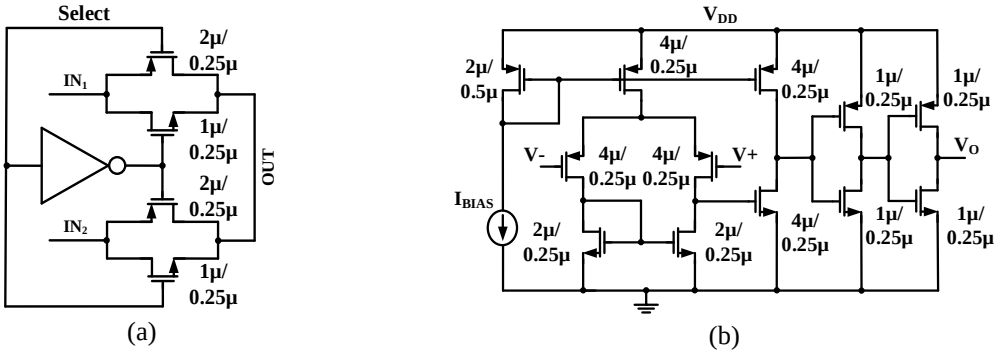

Figure 6. (a) Schematic diagram of Mux 2_1; (b) diagram of the comparator.

$$t_{SS} = \frac{C_{SS} V_{REF}}{I_{BIAS}} \tag{6}$$

3.3. Compensation Circuit

The compensation circuit in this study is of type III, which is often chosen for the converters. Its main task is to ensure that the three modes operate consistently. As shown in Figure 7, type III compensation circuits are widely used in reference literature [20, 21]. It

consists of three capacitors, an amplifier, and a voltage divider resistor. The transfer function can be expressed as shown in equation (7). where V_{REF} is the reference voltage, V_E is the output of the compensator and V_{OUT} represents the output voltage.

$$\frac{V_E}{V_{OUT}} = -\frac{R_1+R_3}{R_1R_3C_3}\frac{\left(s+\frac{1}{R_2C_1}\right)\left(s+\frac{1}{(R_1+R_3)C_3}\right)}{s\left(s+\frac{C_1+C_2}{R_2C_1C_2}\right)\left(s+\frac{1}{R_3C_3}\right)} \tag{7}$$

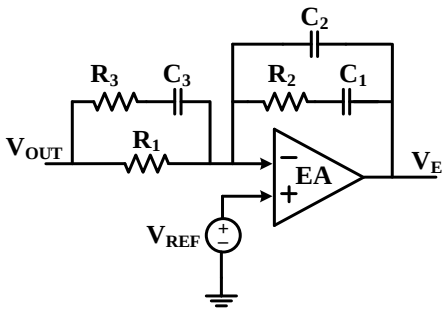

Figure 7. Type-III compensated error amplifier.

3.4. Non-overlapping circuit

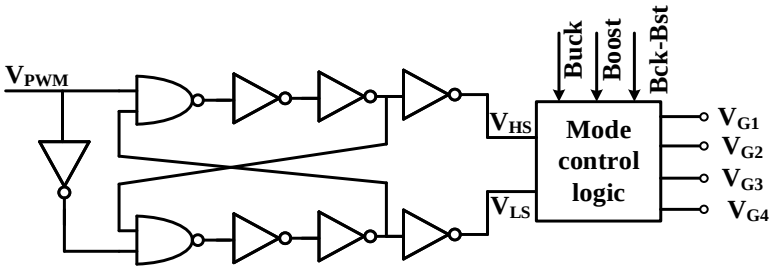

Figure 8. Non-overlapping circuit.

Figure 8 shows a non-overlapping circuit with two main functions: generating duty cycle signals to control the power transistors and preventing them from turning on simultaneously. If all four transistors conduct at once, as illustrated in Figure 2, a large current may flow directly from the V_{IN} to ground, causing excessive power dissipation and potential device failure. The comparator output signal (V_{PWM}) is fed into the circuit, which generates two non-overlapping signals. These are then passed to the mode control logic, producing four non-overlapping gate signals (V_{G1}, V_{G2}, V_{G3}, V_{G4}) to safely drive the four power transistors.

3.5. Ramp generator circuit and bandgap circuit

Figure 9 shows a bandgap voltage reference designed for DC-DC converters, where a stable reference voltage is essential for accurate regulation and high efficiency. The circuit uses three MOSFETs (M_1-M_3), resistors (R_1-R_3), and a current mirror formed by BJTs (Q_1-Q_5) to generate a stable 0.8 V output. Resistor R_0 (1 kΩ) balances current flow, enhancing mirror stability. A differential amplifier between M1 and M2 adjusts transistor operation to maintain

stability under varying temperature and load conditions. By combining PTAT and CTAT voltages, the circuit compensates for temperature changes and provides a reliable, temperature-independent reference, crucial for consistent performance in DC-DC converters.

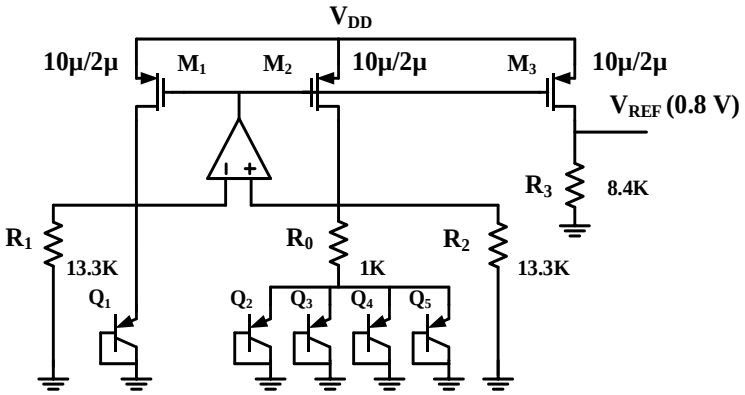

Figure 9. Bandgap circuit.

Figure 10 shows a ramp generator, and a control system based on a comparator, which is often used in DC-DC converters to implement pulse width modulation (PWM). The circuit is controlled by a bias current source that supplies the MOSFET transistors M_1, M_2 and M_3 with a constant current. The transistors M_1 and M_2, together with M_3, generate a ramp voltage across the capacitor C_1, which is used to smooth and shape the ramp signal.

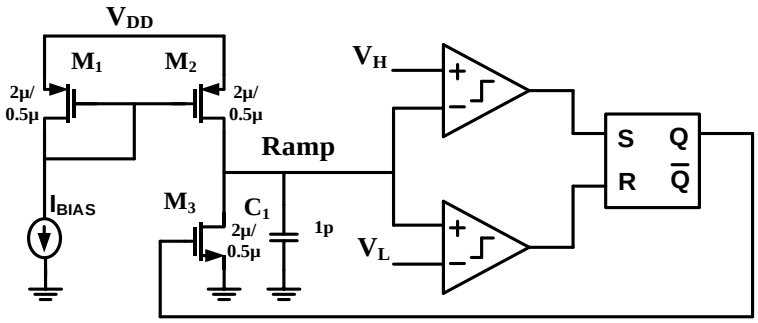

Figure 10. Ramp generator.

The generated ramp signal is fed into two comparators, which compare it with high (V_H) and low (V_L) reference voltages. These control the set (S) and reset (R) inputs of an SR latch, which produces stable digital output signals (Q) for switching the DC-DC converter. This setup enables effective PWM control by adjusting the duty cycle based on the ramp-to-threshold comparison, ensuring accurate voltage regulation and efficient converter operation.

3.6. Control mode logic circuit and driver circuit

The control signals V_{HS}, V_{LS}, V_{G1}, V_{G2}, V_{G3}, and V_{G4}, which control the ON/OFF states of the four power transistors, are determined by the Buck, Boost, and Bck-Bst signals. Based on this logic, the control mode logic circuit (Figure 11) generates appropriate signals for each operating mode, with the SH and SL representing logic high and low, respectively.

Figure 12 shows the driver circuit, consisting of four buffer stages. The transistor length is fixed at 0.25 µm, while the width ranges from 10 µm to 125 µm. To minimize on-resistance, the power transistors are made large. Since the gate nodes have large capacitance, input signals from the control circuit can be distorted, so the driver improves signal strength and switching performance.

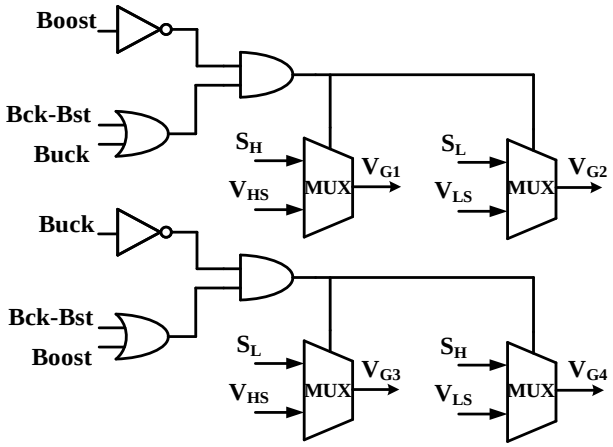

Figure 11. Control mode logic circuit.

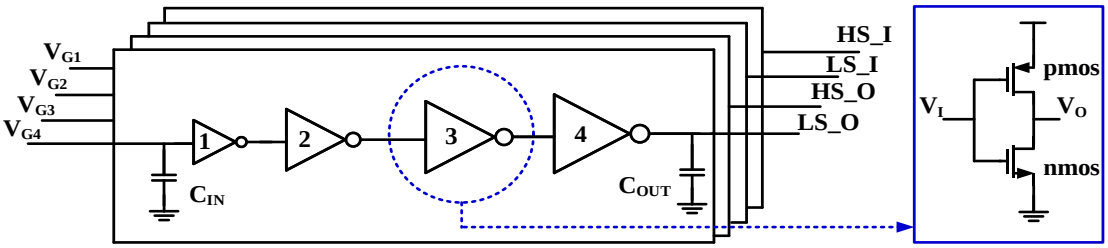

Figure 12. Driver circuit.

3. RESULTS AND DISCUSSIONS

The proposed converter was implemented using a 0.18 µm CMOS process, with a 1 µH off-chip inductor and a 22 µF off-chip capacitor. The converter operates with an input voltage (V_{IN}) from 2.5 V to 5 V, delivers a regulated output voltage (V_{OUT}) of 3.3 V, supports a maximum load current of 800 mA, and switches at 1 MHz. The chip layout (Figure 13) occupies an area of 855 µm × 750 µm. Simulations demonstrate three operating modes. In the Buck mode (Figure 14), M_4 is always ON, M_3 is OFF, and M_1/M_2 switch to regulate the 3.3 V output with a 66% duty cycle when V_{IN} = 5 V. In the Bck-Bst mode (Figure 15), all transistors switch with a 51.5% duty cycle when V_{IN} is approximately equal to V_{OUT}. In the Boost mode (Figure 16), M_1 remains ON, M_2 is OFF, and M_3/M_4 switch to raise V_{IN} = 2.5 V to V_{OUT} = 3.3 V with a 24.4% duty cycle. The converter always starts in the Buck mode, then transitions to the Bck-Bst and finally, the Boost. These transitions may cause minor voltage overshoot, particularly during startup.

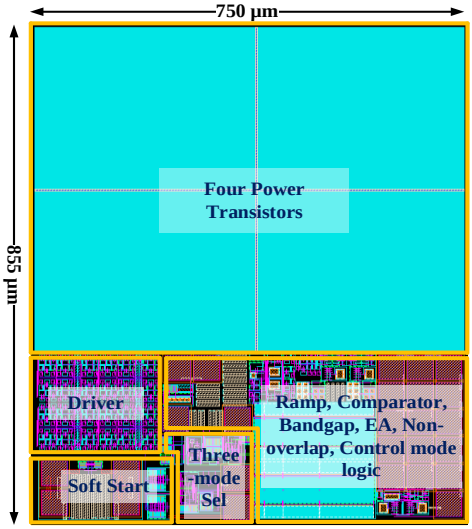

Figure 13. Layout of the converter.

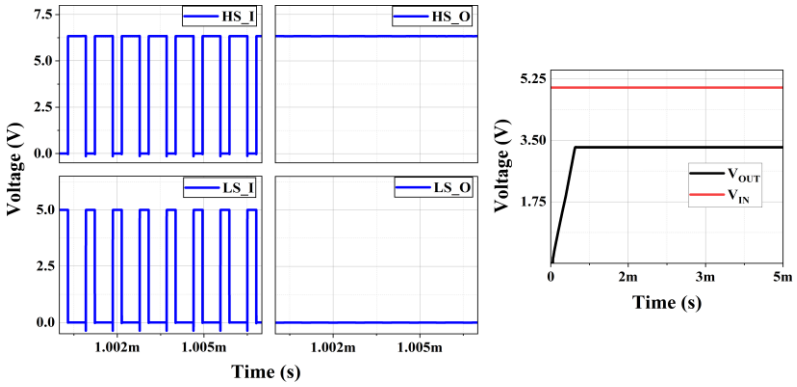

Figure 14. Simulation results in Buck mode with V_{IN} = 5 V and V_{OUT} = 3.3 V.

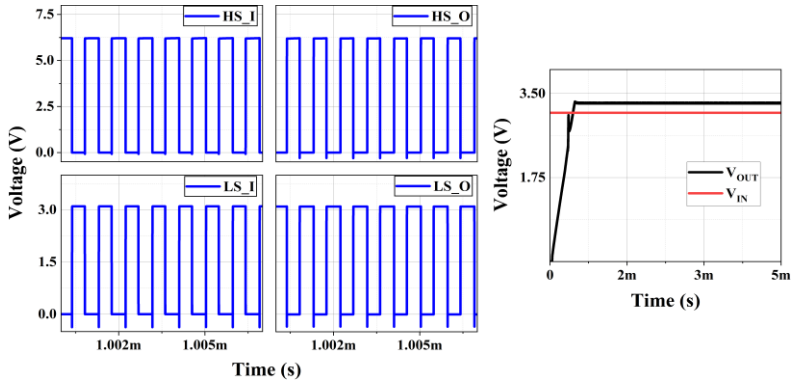

Figure 15. Simulation results in Bck-Bst mode with V_{IN} = 3.1 V and V_{OUT} = 3.3 V.

Figure 17 shows the output voltage response under various temperature and process corners, targeting 3.3 V. In all cases, the output reaches 3.3 V within approximately 550 µs, with slight delays at -40 °C and in the "slow-slow" (ss) corner. The voltage stabilizes with minimal variation, confirming circuit reliability. Figure 18 illustrates the output voltage and current

behavior, showing minor overshoot (up to 3.32 V) and undershoot (down to 3.28 V) during load changes from 0 mA to 800 mA, demonstrating overall stability.

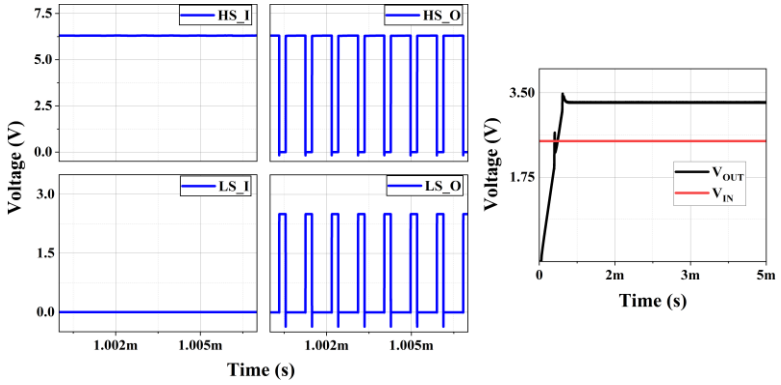

Figure 16. Simulation results in Boost mode with V_{IN} = 2.5 V and V_{OUT} = 3.3 V.

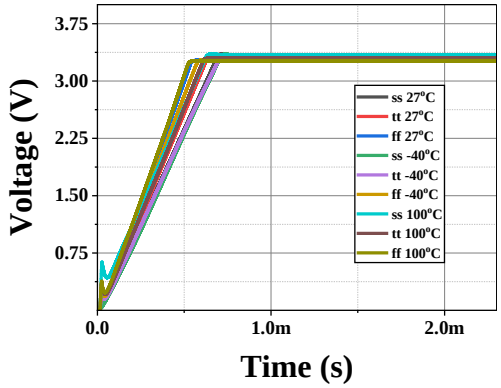

Figure 17. Output voltage response across process corners and temperature conditions.

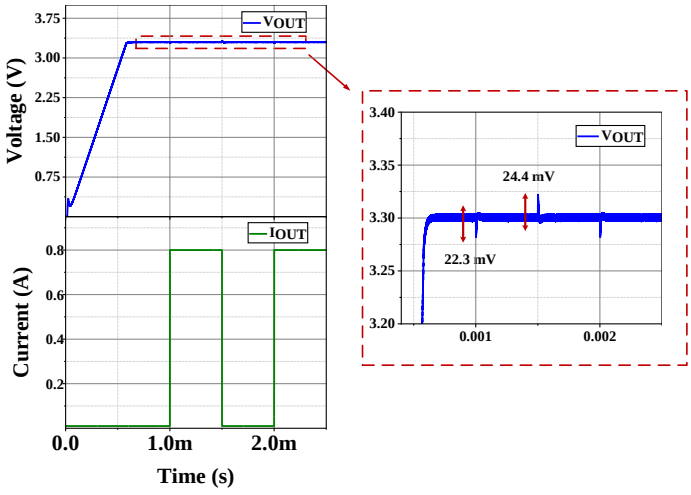

Figure 18. Output voltage and current response of the converter.

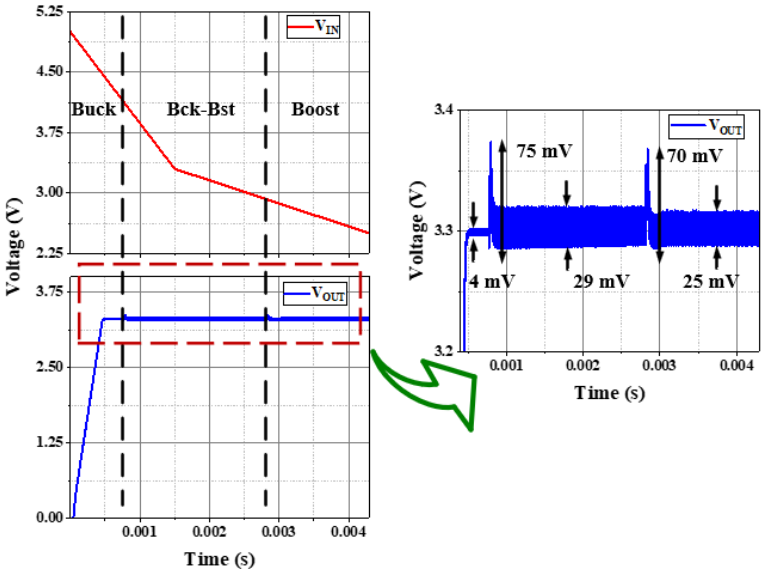

Figure 19. Converter's voltage rippled over the entire operating range.

Table 1. Performance Summary and Comparison with Other Converters.

Parameter	[13]	[16]	[15]	[14]	[22]	This work
Technology (nm)	65	180	--	180	180	180
Modes	C	B	A	C	B	B
Efficiency (%)	72	94.8	85.5	91	78	95.6
Frequency (MHz)	35	3.2	1	5	0.2	1
Input Range (V)	1.2 - 3.6	3 - 8	2.5 - 4.5	2.5 - 4.5	1.5 - 3.5	2.5 - 5
Output (V)	1.5 - 1.8	5	3.3	2 - 4	0.6 - 2.3	3.3
Max. I_{LOAD} (A)	0.007	0.5	0.5	0.4	0.004	0.8
Results	Sim.	Mes.	Mes.	Mes.	Sim.	Sim.

A: Mode Bck-Bst; B: Mode Buck, Boost and Bck-Bst; C: Mode Buck and Boost.

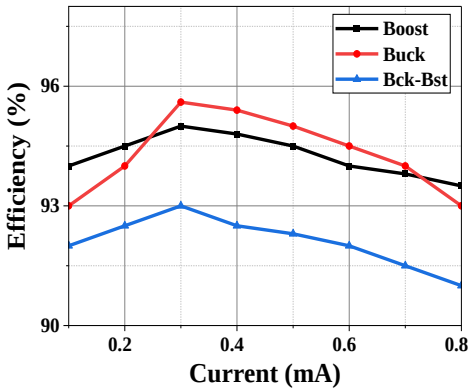

Figure 20. Efficiency of the converter.

Figure 19 shows the converter operating in Boost, Buck, and Bck-Bst modes over a V_{IN} range of 2.5 - 5 V, with voltage ripples of 4 mV, 29 mV, and 21 mV, respectively, and an overshoot of 75 mV during mode transitions. Figure 20 illustrates the efficiency under 100 mA and 800 mA loads, demonstrating consistently high performance across input voltages. Table 1 compares the proposed converter with previous works, highlighting its triple-mode operation for output regulation, high efficiency up to 95.6 %, and low no-load power consumption (500 µW - 1 mW), outperforming efficiencies of 72 %, 91 %, 85.5 %, 94.8 %, and 78 % reported in [13 - 16, 22]. The design supports up to 800 mA output, making it suitable for medium-power, battery-operated applications.

4. CONCLUSIONS

The proposed converter is well-suited for battery-powered applications requiring high efficiency and extended battery life. Its three-mode control (Buck, Bck-Bst, Boost) enables seamless switching with stable performance. A soft-start circuit enhances reliability by limiting inrush current. Implemented in 0.18 µm CMOS, the design maintains a stable 3.3 V output across a 2.5 - 5 V input and supports 100 - 800 mA load currents. The chip occupies 855 µm × 750 µm and achieves up to 95.6 % efficiency.

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